L Number	Hits	Search Text	DB	Time stamp
1	1534	708/620-632.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/19 14:42
2	752	708/620-632.ccls. and shift$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/19 14:42
3	190	(708/620-632.ccls. and shift$3) and counter$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/19 14:42
4	120	((708/620-632.ccls. and shift$3) and counter$1) and (shift$3.ti. or shift$3.ab. or shift$3.clm.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/19 14:43
5	23	(((708/620-632.ccls. and shift$3) and counter$1) and (shift$3.ti. or shift$3.ab. or shift$3.clm.)) and counter$1.clm.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/19 14:43
-	1903	Rong.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:25
-	39053	Lin.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:26
-	152	Rong.in. and Lin.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:26
-	34	(Rong.in. and Lin.in.) and multipl$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:28
-	22167	708/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:29
-	6694	708/$.ccls. and power$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:29
-	5435	(708/$.ccls. and power$1) and multipl$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:29
-	2789	((708/$.ccls. and power$1) and multipl$7) and adder$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:30
-	1214	(multipl$7.ti. or multipl$7.ab.) and (((708/$.ccls. and power$1) and multipl$7) and adder$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:31

-	320	((multipl$7.ti. or multipl$7.ab.) and (((708/$.ccls. and power$1) and multipl$7) and adder$1)) and (power$1.ti. or power$1.ab. or power$1.clm.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:31
-	54	(((multipl$7.ti. or multipl$7.ab.) and (((708/$.ccls. and power$1) and multipl$7) and adder$1)) and (power$1.ti. or power$1.ab. or power$1.clm.)) and matri$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:44
-	73	708/607.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:45
-	169	708/607,700.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:45
-	67	708/607,700.ccls. and power$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:45
-	62	(708/607,700.ccls. and power$1) not ((((multipl$7.ti. or multipl$7.ab.) and (((708/$.ccls. and power$1) and multipl$7) and adder$1)) and (power$1.ti. or power$1.ab. or power$1.clm.)) and matri$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:45
-	53	multipl$7 and ((708/607,700.ccls. and power$1) not ((((multipl$7.ti. or multipl$7.ab.) and (((708/$.ccls. and power$1) and multipl$7) and adder$1)) and (power$1.ti. or power$1.ab. or power$1.clm.)) and matri$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/12 09:45

Fast multiplier schemes using large parallel counters and shift switches

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Abstract:
We present novel fast parallel multiplier schemes. In contrast to the full adder binary logic based traditional designs, we use (incomplete) large parallel counters and large shift switch compressors, which are built based on shift switch logic, a logic with shift switches as logic elements performing modulo arithmetic operations on (non-binary) state signals. With the unique feature of shift switch logic our parallel multiplier schemes have shown superiority in speed and in area compactness. This is provided through the use of a stage-reduced partial product reduction network, the efficient signal interconnection and the simplified final carry lookahead adder. Compared to the well-known designs, our approach possesses higher regularity and simplicity on circuit structures, characterized by both the recursive shift switch networks which localize the major part of partial product reduction and the deliberated utilization of uneven arrival signals which minimize the delay of the multipliers

Index Terms:
adders carry logic circuit optimisation counting circuits delays digital arithmetic logic design minimisation multiplying circuits shift registers area compactness carry lookahead adder fast parallel multiplier schemes full adder binary logic large parallel counters large shift switch compressors logic elements modulo arithmetic operations multiplier delay minimization partial product reduction recursive shift switch networks shift switch logic signal interconnection speed stage-reduced partial product reduction network state signals uneven arrival signals